What is claimed is:

1. A spread spectrum demodulator for demodulating a plurality of received spread spectrum signals, comprising:

a timing detector for receiving amplitude components of the plurality of received spread spectrum signals, the amplitude components being produced by de-spreading and then polar-coordinates-converting the spread spectrum signals, establishing initial synchronization individually for the spread spectrum signals by detecting maximum values of the amplitude components, and outputting individually traced pieces of reception timing of the spread spectrum signals; and

a plurality of correctors for latching, with the pieces of reception timing that are outputted from said timing detector, a plurality of frequency components of the respective spread spectrum signals, the frequency components being produced by de-spreading and then polar-coordinates-converting the spread spectrum signals, and correcting for an offset, and outputting resulting signals.

2. The spread spectrum demodulator according to claim 1, wherein said timing detector comprises:

an amplitude judgment section for receiving the amplitude components of the plurality of received spread spectrum signals and detecting timing by threshold judgment;

a masking section for masking timing detected by said amplitude judgment section when the timing is within a predetermined range of already detected timing, and for outputting only so far undetected timing;

a timing judgment section for outputting, as initial synchronization timing, the so far undetected timing inputted from said masking section;

a plurality of tracing sections for storing the initial synchronization timing inputted from said timing judgment section and tracing the timing

until a spread spectrum signal corresponding to the initial synchronization timing ceases; and

a masking condition section for outputting pieces of timing being traced by said respective tracing sections to said masking section.

3. The spread spectrum demodulator according to claim 2, wherein each of said tracing sections comprises:

a comparison section for outputting, as first reception timing, the initial synchronization timing inputted from said timing judgment section, comparing amplitudes inputted from said amplitude judgment section by a timing that is within a predetermined timing of a delayed timing from the first reception timing, and outputting, as reception timing, timing having a maximum amplitude; and

a delay storage section for storing the reception timing outputted from said comparison section and outputting it to said comparison section after delaying it by a predetermined time.

4. The spread spectrum demodulator according to claim 3, wherein the length of the reception timing stored in said delay storage section is a one-symbol timing length.

5. The spread spectrum demodulator according to claim 4, wherein the predetermined range of already detected timing masked by said masking section is within a 0.5 chip timing before and after the already detected timing.

6. The spread spectrum demodulator according to claim 5, wherein said masking condition section is an logical OR circuit.

7. The spread spectrum demodulator according to claim 4, wherein said masking condition section is an logical OR circuit.

8. The spread spectrum demodulator according to claim 3, wherein the predetermined range of already detected timing masked by said masking section is within a 0.5 chip timing before and after the already detected timing.

9. The spread spectrum demodulator according to claim 8, wherein said masking condition section is an logical OR circuit.

10. The spread spectrum demodulator according to claim 3, wherein said masking condition section is an logical OR circuit.

11. The spread spectrum demodulator according to claim 2, wherein the predetermined range of already detected timing masked by said masking section is within a 0.5 chip timing before and after the already detected timing.

12. The spread spectrum demodulator according to claim 11, wherein said masking condition section is an logical OR circuit.

13. The spread spectrum demodulator according to claim 2, wherein said masking condition section is an logical OR circuit.